What is claimed is:

1. A method for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed; and

inducing a detectable response from the exposed region as a function of a portion of the circuitry and, therefrom, analyzing the die.

2. The method of claim 1, wherein inducing a detectable response includes using an electron beam.

3. The method of claim 2, further including detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and wherein analyzing the die includes using a scanning electron microscope (SEM).

4. The method of claim 3, wherein analyzing the die includes detecting a first magnitude of secondary electrons from a selected circuit portion and a second magnitude of secondary electrons detected from another circuit portion, the first and second magnitudes of secondary electrons being indicative of an electric characteristic differential between the selected circuit portion and the other circuit portion.

5. The method of claim 4, further comprising detecting secondary electrons from a plurality of circuit portions and obtaining an image of the die that represents variations in voltage across the plurality of circuit portions.

6. The method of claim 2, wherein using the electron beam includes pulsing the beam, and wherein analyzing the die includes obtaining a waveform response to the pulsed beam.

7. The method of claim 6, further comprising coupling a power supply to the die and inputting electrical signals to the die to generate a response.

8. The method of claim 1, wherein inducing a detectable response includes inducing a response as a function of an electrical characteristic of a source/drain region in the die.

9. The method of claim 1, wherein inducing a detectable response includes using a buried oxide (BOX) portion of the SOI structure as a dielectric.

10. The method of claim 9, wherein removing a portion of substrate from the back side of the semiconductor die includes exposing a portion of the BOX.

11. The method of claim 1, wherein analyzing the die includes post-manufacturing analysis.

12. The method of claim 11, wherein analyzing the die includes obtaining a response for electrical stimulus applied to circuitry in the die.

13. The method of claim 12, wherein inputting electrical signals includes inputting signals known to induce a failure in the die.

14. The method of claim 12, wherein inputting electrical signals includes inputting signals in a continuous loop.

15. The method of claim 1, further comprising inducing a detectable response from a non-defective die in the same manner as the die being analyzed, the non-defective die having the same design as the die being analyzed, and comparing the analysis of the dies.

16. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the system comprising:

means for removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed;

means for inducing a detectable response from the exposed region as a function of a portion of the circuitry; and

means for detecting the response and, therefrom, analyzing the die.

17. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the system comprising:

a substrate removal arrangement adapted to remove substrate from the back side of the semiconductor die and expose a region of the insulator of the SOI structure where the portion has been removed;

a probe arrangement adapted to induce a detectable response from the exposed region as a function of a portion of the circuitry; and

a detector adapted to detect the response and, therefrom, analyze the die.

18. The system of claim 17, further comprising a controller adapted to control the substrate removal arrangement.

19. The system of claim 18, wherein the controller is adapted to control the substate removal arrangement to remove sufficient substrate to facilitate the inducing of a response from the exposed region as a function of a portion of the circuitry.

20. The system of claim 17, wherein the substrate removal arrangement is adapted to remove enough substrate to expose a BOX portion of the SOI structure.

21. The system of claim 17, wherein the probe arrangement includes an SEM adapted to provide at least one of: an image of a circuit under analysis and data for probe navigation.

22. The system of claim 21, wherein the SEM also includes the detector and is further adapted to obtain an image of the die having light and dark areas, the dark areas being indicative of circuit portions having a positive voltage greater than that of lighter areas.

23. The system of claim 17, further comprising a tester adapted to introduce electrical stimulus to the die.